Amendments to the Specification:

The applicant has cancelled the term "two-system interfaces" according to the examiner's suggestion and returned it back to its original term "double configuration connector interface." Both of terms express an interface with two different kinds of outputs to the system end. As such, no substantive changes or additions are embodied, and the amendments do not add any new matter to this application.

Please substitute the following amended paragraph for paragraph 0007:

[0007] In one embodiment, the multiple format interface adapter for small storage media comprises a casing, a ~~two system-end interfaces~~ double-configuration connector interface, a reversed U-shape slot and a circuit board. The ~~two system-end interfaces~~ double-configuration connector interface is mounted at a front of the casing to insert in and connect to a system end. The reversed U-shape slot has a Compact Flash (CF)-interface and formed at a rear end of the adapter by guide tracks that are located at sides of the Compact Flash (CF) interface. The circuit board is arranged between the ~~two system-end interfaces~~ double-configuration connector interface and the Compact Flash (CF) interface. A signal converter control chip connected between the ~~two system-end interfaces~~ double-configuration connector interface and the Compact Flash (CF) interface, wherein the signal converter control chip is configured to control signal conversion and signal transmission between the system end and the CompactFlash format storage medium.

Please substitute the following amended paragraph for paragraph 0008:

[0008] The Compact Flash (CF) interface includes at least one Compact Flash (CF) card detect pin. The ~~two system-end interfaces~~ double-configuration connector interface includes a card insertion detect pin to detect the insertion of any Compact Flash (CF) format storage media. The system end provides a work voltage according to an enable signal transmitted from the ~~two system-end interfaces~~ double-configuration connector interface to allow the adapter transmitting different types of electronic signal for controlling the data reading/writing operation.

Please substitute the following amended paragraph for paragraph 0009:

[0009] In another embodiment, the ~~two system-end interfaces~~ double-configuration connector interface comprises a PCI Express interface and a USB interface. The signal converter control chip is an IDE converter control chip configured to convert CompactFlash format storage medium-compatible USB signals to system-compatible IDE signals. The slot also accommodates various types of small memory cards. The ~~two system-end interfaces~~ double-configuration connector interface includes a plurality of card insertion detect pins to detect the insertion of various types of the memory cards. A signal converter is mounted in the casing to correspond to the slot for signal transmission between the ~~two system-end interfaces~~ double-configuration connector interface and the system end when the small memory cards insert through the slot.

Please substitute the following amended paragraph for paragraph 0021:

[0021] In the illustrated embodiment, the multiple format interface adapter for small storage media is exemplary suitable for the specification of Compact Flash ("CF") Card. The multiple format interface adapter for small storage media includes an assembly of first and second case bodies 10, 11, a ~~two system-end interfaces~~ double-configuration connector interface 14, a Compact Flash (CF) interface 16, a circuit board 18, and IDE converter control chip 182 connected on the circuit board 18.

Please substitute the following amended paragraph for paragraph 0022:

[0022] The ~~two system-end interfaces~~ double-configuration connector interface 14 is coupled with a system end at a front of the case bodies 10, 11. A rear of the case bodies 10, 11 respectively forms a reversed U-shape 13 with side guide tracks 12, at a side of which is placed the Compact Flash (CF) interface 16. The Compact Flash (CF) interface 16 is mounted at an end of the guide tracks 12 adjacent to the ~~two system-end interfaces~~ double-configuration connector interface 14. A Compact Flash (CF) format storage medium is inserted along the guide tracks 12 to connect to the Compact Flash (CF)-interface 16.

Please substitute the following amended paragraph for paragraph 0023:

[0023] The ~~two system-end interfaces~~ double-configuration connector interface 14 and the Compact Flash (CF) interface 16 are connected each other via a circuitry carried by the circuit board 18. The circuit board 18 includes the connection of the IDE converter control chip 182 compatible with Compact Flash (CF) format devices. The chip 182 is operable to convert IDE standard signals to USB standard signals between

an external system terminal and the Compact Flash (CF) format storage medium. A Compact Flash (CF) card is compatible with three operating modes, i.e. a memory mode, I/O mode, and a true IDE mode. In the illustrated embodiment, the Compact Flash (CF) format storage medium is used as an external hard disk vis-à-vis the system end. The Compact Flash (CF) format storage medium in this embodiment therefore has pins that correspond to the true IDE mode of the IDE interface, being implemented as control interface for signal transmission.

Please substitute the following amended paragraph for paragraph 0024:

[0024] As shown in FIG. 2, the Compact Flash (CF) format storage medium can be a removable Compact Flash (CF) memory card or a micro-drive 20. As shown in FIG. 3, the Compact Flash (CF) format storage medium can alternatively be a fixed small hard disk 30.

Please substitute the following amended paragraph for paragraph 0025:

[0025] In the embodiment of FIG. 4, the ~~two system-end interfaces~~ double-configuration connector interface 14 is specifically compatible with Express Cards, the Compact Flash (CF) format interface 16 is specifically compatible with Compact Flash (CF) format storage media, and the IDE converter control chip 182 operates as a signal control core.

Please substitute the following amended paragraph for paragraph 0026:

[0026] The ~~two system-end interfaces~~ double-configuration connector interface 14 includes two signal transmission formats, which can be a PCI Express interface and a USB interface. According to the design requirement, either the PCI Express interface

or the USB interface can be implemented as an operating interface. In the illustrated embodiment, the ~~two system-end interfaces~~ double-configuration connector interface 14 exemplary operates as a USB interface.

Please substitute the following amended paragraph for paragraph 0027:

[0027] The Compact Flash (CF) format interface 16 includes a Compact Flash (CF) card detect pins 25 (nCD2), 26 (nCD1). The ~~two system-end interfaces~~ double-configuration connector interface 14 includes a card insertion detect pin 4 (CPUSB# which is belonged to USB interface, wherein "#" means a "Low-Active" pin) connected to the Compact Flash (CF) card detect pins 25, 26 for detecting the insertion of a Compact Flash (CF) format storage medium. The pins 25, 26, 4 are Low-Active pins, i.e. they are at low potential when a Compact Flash (CF) format storage medium is connected, and the card insertion detect pin 4 (CPUSB#) provides a card insertion-enable signal to the system end. The ~~two system-end interfaces~~ double-configuration connector interface 14 also includes power terminals 14, 15. When the card insertion detect pin 4 (CPUSB#) is in an enabled status, the system end transmits an operating voltage to the adapter so that its internal electronic components can start data reading required for the system.

Please substitute the following amended paragraph for paragraph 0028:

[0028] In an embodiment where the USB interface is implemented for data reading, the IDE converter control chip 182 has two sets of system data transmission pins, i.e. (HU_DP(3), HU_DM(5)) and (U_DP(2), U_DM(4)) pins respectively needed for high-speed USB (transmission rate of about 480Mbps) and full-speed USB

(transmission rate of about 12Mbps). The ~~two system-end interfaces~~ double-configuration connector interface 14 has a set of differential serial pins 2, 3 connected to the system data transmission pins. In particular, the pin USB_D- is connected to HU_DM(5) and U_DM(4), and the pin USB_D+ is connected to HU_DP(3) and U_DP(2). Via the foregoing connection scheme, transmission operations can be performed, including address transmission, data transmission, and control signal transmission.

Please substitute the following amended paragraph for paragraph 0029:

[0029] Within the multiple format interface adapter for small storage media, signal transmission is performed in parallel. The Compact Flash (CF) format interface 16 includes address pins (A00~A02), data transmission pins (D00~D15), and control pins (RESET, nIOWR, nIORD, nWAIT, IREQ, nCE1, nCE2, nSPKR). The IDE converter control chip 182 includes address pins (DA0~DA2), data transmission pins DD0~DD15), and control pins (RESET-, DIOW-, DIOR-, IORDY, INTRQ, CS0-, CS1-, DASP-).

Please substitute the following amended paragraph for paragraph 0031:

[0031] FIG. 5 is a schematic view of a multiple format interface adapter for small storage media a plurality of memory cards according to an embodiment of the invention. The multiple format interface adapter for small storage media includes the assembly of a casing 50, a ~~two system-end interfaces~~ double-configuration connector interface 54, a signal [[a]] converter 56, a circuit board 58 and a multi-card reader control chip 582 connected on the circuit board 58.

Please substitute the following amended paragraph for paragraph 0032:

[0032] The ~~two system-end interfaces~~ double-configuration connector interface 54 is assembled at a front of the casing 50, while a slot 502 is formed at a rear of the casing 50 for insertion of small memory cards. The signal converter 56 is placed inside the casing 50 at a location corresponding to the area of the slot 502. The signal converter 56 can receive the placement of a small memory card through which signal transmission is performed via the ~~two system-end interfaces~~ double-configuration connector interface 54 with the system end. The signal converter 56 can be divided into three structural parts, which include an upper layer for configuring SM/xD contact pins (not shown), an accommodating space 562 for receiving the placement of the memory card, and a lower layer for configuring MS type memory card contact pins 566 and SD/MMC memory card contact pins 564. SM/xD contact pins and MS and SD/MMC contact pins 566, 564 can be interchangeably placed on the upper and lower layers. If there is a sufficient space, all the connection contact pins can be also placed on a same level to obtain a thinner signal converter 56.

Please substitute the following amended paragraph for paragraph 0033:

[0033] The multi-card reader control chip 582 and the circuit board 58 are connected between the ~~two system-end interfaces~~ double-configuration connector interface 54 and the signal converter 56. The circuit board 58 and the multi-card reader control chip 582 operate as a signal controller between an outer system and the small memory card.

Please substitute the following amended paragraph for paragraph 0036:

[0036] A PCI Express interface or a USB interface can be implemented with the adapter of the invention. In this embodiment, the ~~two system-end interfaces~~ double-configuration connector interface is a USB interface, and the multi-card reader control chip 582 is configured to convert the parallel transmission signals from the memory cards into USB serial signals.

Please substitute the following amended paragraph for paragraph 0037:

[0037] Similar to the foregoing description, the multi-card reader control chip 582 has two sets of system data transmission pins, i.e. USB_HDP(4), USB_HDM(5) and USB_FDP(3), USB_FDM(6) pins respectively needed for high-speed USB (transmission rate of about 480Mbps) and full-speed USB (transmission rate of about 12Mbps). The ~~two system-end interfaces~~ double-configuration connector interface 54 has a set of differential serial pins 2, 3 connected to the system data transmission pins (i.e. USB_D- is connected to USB_HDM(5), USB_FDM(6), and USB_D+ is connected to USB_HDP(4), USB_FDP(3)). Via this connection scheme, signal transmission including address signals, data signals and control signals is performed with the external system.

Please substitute the following amended paragraph for paragraph 0038:

[0038] Referring to FIG. 7-8, the ~~two system-end interfaces~~ double-configuration connector interface 54 has a card insertion detect pin 4 (CPUSB#) for detecting the connection of a memory card. The signal converter 56 has a card detect pin 23 (CD_SW1) corresponding to a first type of memory card (for example SM/xD), a second card detect pin 6 (INS) corresponding to a second type of memory card (for example

MS), and a third card detect pin 10 (CD_SW#) corresponding to a third type of memory card (for example SD/MMC). The multi-card reader control chip 582 has a first detect pin 22 (SM_CD_SW#), a second detect pin 30 (MS_INS#) and a third detect pin 37 (SD_CD_SW#), through which the multi-card reader control chip 582 detects the connection of memory card.